(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 January 2004 (08.01.2004)

PCT

(10) International Publication Number
WO 2004/003882 A1

(51) International Patent Classification[7]: G09G 3/36

(21) International Application Number: PCT/EP2003/006638

(22) International Filing Date: 23 June 2003 (23.06.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
MI2002A001424 27 June 2002 (27.06.2002) IT

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(81) Designated States *(national)*: CN, IN, JP, US.

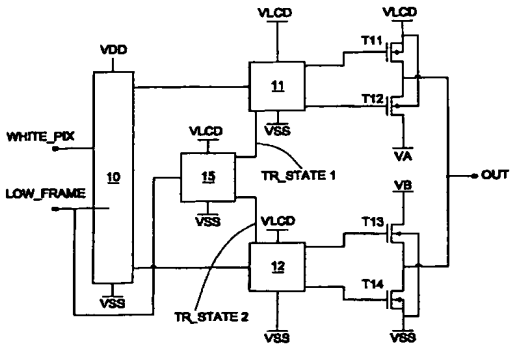
(84) Designated States *(regional)*: European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR).

Declarations under Rule 4.17:
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for the following designation US*
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM FOR DRIVING COLUMNS OF A LIQUID CRYSTAL DISPLAY



(57) Abstract: The present invention refers to a system for driving columns of a liquid crystal display comprising a logic circuitry (10) operating in a supply path between a first (VDD) and a second (VSS) supply voltage in which the first supply voltage is (VDD) higher than the second supply voltage (VSS). The logic circuitry (10) is capable of generating starting from the first logic signals (LOW_FRAME, WHITE_PIX) in input second logic signals (CP, CN, CP_N, CN_N) in output whose value is equal to the first (VDD) or second (VSS) supply voltage. The device comprises two elevator devices (11, 12) coupled to the logic circuitry (10) and operating in a supply path between a third supply voltage (VLCD) greater than the first supply voltage (VDD) and the second supply voltage (VSS); the elevator devices (11, 12) are capable of raising the value of the second logic signals (CP, CN, CP_N, CN_N). The device also comprises a first (T11-T12) and a second (T13-T14) pair of transistors shaving different supply paths (VLCD-VA, VB-VSS) and having an output terminal (OUT) in common; the first (T11-T12) and the second (T13-T14) pair of transistors are connected to the elevator devices (11, 12) so as to determine the drive signal of a column. The device comprises turnoff circuitry (15) operating in a supply path between the third (VLCD) and the second supply voltage (VSS) and coupled to the two elevator devices (11, 12). The circuitry (15) is capable of keeping one of the two pairs of transistors (T11-T12, T13-T14) in a turnoff state in the period of time of a frame when the other of the two pairs of transistors (T11-T12, T13-T14) is in operative conditions.

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"System for driving columns of a liquid crystal display."

DESCRIPTION

* * * *

The present invention refers to a system for driving columns of a liquid crystal display.

Liquid crystal displays (LCD) are used today in an ever-increasing number of products such as cellular telephone, portable computers, etc. The displays, that can be in black and white, in a grey or colours scale, are usually made up of a matrix of electrodes in rows and columns which, appropriately driven by means of the application of a voltage signal, cause at the crossing points, the so-called pixels, a change in optic behaviour of the liquid crystal placed between.

The image that is visualized on the display is obtained through different possible methods for driving the rows and the columns.

One method that is often used for driving an LCD and is known as Improved Alt & Pleshko (IA&P) requires a single row electrode to be excited for an elementary period of time by means of a single selection pulse and the simultaneous excitation of the column electrodes; to the latter are then applied voltage values suitable for causing all the pixels that belong to that single row to be turned on or turned off. For a successive period of elementary time there will be the excitation of another row electrode and so on until the scanning of the last row electrode is completed; therefore if the row electrodes are a number N and T is the period of elementary time, the time needed for scanning all the rows will be given by NT which is also called "frame".

The optic transmission characteristics of the liquid crystal vary with the amplitude of the voltage applied to the relative pixel, but the application of direct voltage is damaging for the liquid crystal as it permanently changes and degrades the physical properties of the material. For this reason the voltage signals used to drive the single pixels of an LCD are alternating

voltage in relation to a common value of direct voltage that not necessarily has to be the ground potential. In this manner the driving of a pixel of the display comes about through two waveforms of equal amplitude but with opposite polarity in relation to a common voltage, that follow each other periodically. Therefore the driving voltage applied to a given pixel during its period T within a frame is applied with opposite polarity during the respective period T of the successive frame.

Nevertheless all these voltage transitions involve a significant power that has to be managed by the drive circuits. Therefore one of the primary purposes in planning the driving devices of LCD rows and columns is to reduce the power consumption so as to minimise both the power delivered by the power supplies of said devices, and the power dissipated by them.

One part of a driving device of LCD rows and columns, more precisely the Philips PCF8548 device, is described in Figure 1.

The LOW_FRAME signal is a logic signal that equals 0 in the even frames, and equals 1 in the uneven frames. WHITE_PIX is instead a logic signal that equals 0 when the pixel has to be on, equalling 1 when the pixel has to be kept off. Starting from these two signals are generated, through a circuit 1, the control signals that drive two transistors PMOS T9, T10 and two transistors NMOS T7, T8.

In particular the gate terminals of the transistors T8, T9 and T10 are driven through 3 identical circuit cells C1, shown in Figure 2. Said cells are level-shifters that is buffers that convert the logic signal levels from low voltage to high voltage in particular from the supply voltage VDD to a driving voltage VLCD generated by a device (not shown in the Figure) comprising a booster regulator through the connection of a certain number of stages of a charge pump.

Each cell C1 comprises two transistors NMOS M22 and M23 driven by the signals A and NA, the output signal of the logic circuitry 1 and the negated signal A. The source terminals of the transistors M22 and M23 are

connected to the voltage VSS and the drain terminals are connected respectively to the drain terminals of two transistors PMOS M20 and M21 on the source terminal of which the voltage VLCD is present; in addition the drain terminals of the transistors M22 and M23 are connected to the gate terminals of the transistors M21 and M20. The outputs Q drive the gate of the transistors T10, T9 and T8.

The gate terminal of the transistor T7 is instead driven directly by a logic low voltage signal.

The source terminal of the transistor T9 is connected to a voltage reference VA while the drain terminal is connected to the drain terminal of the transistor T10 whose source terminal is connected to the voltage VLCD. The source terminal of the transistor T8 is connected to a voltage reference VB while the drain terminal is connected to the drain terminal of the transistor T7 whose source terminal is connected to the voltage VSS. The drain terminals of the pairs of transistor T7-T8 and T9-T10 are in common and supply the output signal OUT.

The voltages VA and VB are different levels of intermediate voltages between the voltages VLCD and VSS that are generated inside the drive device of an LCD. The relation between these levels and VLCD is chosen on the basis of the dimension of the matrix of the display according to the criteria that will be shown below.

In particular according to the technique of Improved Alt & Pleshko, to drive the liquid crystal display adequately, four different voltage levels intermediate between VLCD and VSS are generated inside the device. The relation between these and VLCD is set on the basis of the number of rows m of the display according to the relations:

VLCD, [(n+3)/(n+4)]*VLCD, [(n+2)/(n+4)]*VLCD, [2/(n+4)]*VLCD, [1/(n+4)]*VLCD, VSS)

with n given by the square root of m-3.

If, for example, m = 81 => n = 6 in the case of a display with 81 rows

the voltage levels will be:

VLCD (9/10)*VLCD (8/10)*VLCD (2/10)*VLCD (1/10)*VLCD VSS.

With reference to the drive circuit of Figure 1, in the case of a drive of columns, the voltage references VA and VB will be equal respectively to (8/10)*VLCD and (2/10)*VLCD. The drive will come about, for example, in the following manner: in a frame the transistors T9 and T10 will be turned on alternately while T7 and T8 will be off; in this case the output signal OUT, suitable for driving a column, will vary between VLCD and VA according to whether the corresponding pixel on the matrix of rows and columns given at the crossing point of the column and the row is on or not. In the successive frame the transistors T7 and T8 will be turned on alternately while the transistors T9 and T10 will be off and therefore the output signal will vary between VSS and VB according to whether the pixel of the crossing point of the corresponding column and row will be on or not. The wave forms of the output signal OUT in the case of driving two columns COL0 and COL1 for a frame n and for the successive frame n+1 are shown in Figure 3. The Figure 4 shows the image as it appears on the display.

In view of the state of the technique, the object of the present invention is to produce a system for driving columns of a liquid crystal display that has minor consumption of current in comparison to known devices.

In accordance with the present invention, this object is achieved by means of a system for driving columns of a liquid crystal display comprising a logic circuitry operating in a supply path between a first and a second supply voltage with first said supply voltage higher than said second supply voltage, said logic circuitry being capable of generating starting from first logic signals in input second logic signals in output whose value is equal to said first or second supply voltage, elevator devices coupled to said logic circuitry and operating in a supply path between a third supply voltage

greater than said first supply voltage and said second supply voltage, said elevator devices being capable of raising the value of said second logic signals, a first and a second pair of transistors having different supply paths and having an output terminal in common, said first and second pairs of transistors being associated to said elevator devices and to said logic circuitry so as to determine the drive signal of a column, characterised in that said elevator devices are two and each of them is connected with one of said pairs of transistors, and in that it comprises a turnoff circuitry coupled to said two elevator devices, said circuitry being capable of keeping one of the two pairs of transistors in the turnoff state in the period of time of a frame when the other of said two couples of transistors is in operative conditions.

The characteristics and the advantages of the present invention will appear evident from the following detailed description of an embodiment thereof illustrated as non-limiting example in the enclosed drawings, in which:

Figure 1 is a circuitry diagram of a driving device of columns of an LCD according to the known art;

Figure 2 is a more detailed circuitry diagram of a part of the circuit of Figure 1;

Figure 3 shows waveforms of the output voltage signal of the circuit of Figure 1 in the case of driving two columns;

Figure 4 shows an image formed on the display of an LCD;

Figure 5 is a circuitry diagram of a system for driving the columns of an LCD according to the invention;

Figure 6 is a more detailed circuitry diagram of the device of Figure 5;

Figure 7 shows the temporal waveforms LOW_FRAME, WHITE_PIX, CN, CN_N, CP, CP_N and OUT concerning the circuit of Figure 6.

Figure 5 shows a circuit diagram of a system for driving columns of an LCD according to the present invention. Said device comprises a low

voltage logic circuit 10 operating between a supply voltage VDD and a supply voltage VSS, two level-shifters 11 and 12 operating between a supply voltage VLCD supplied by a device comprising a booster regulator through the connection of a certain number of stages of a charge pump and the voltage VSS, a pair of transistors PMOS T11, T12 and a pair of transistors NMOS T13, T14 having different supply paths. The principle on which the invention is based is that in a frame there will never be both the transistors PMOS T11, T12 or both the transistors NMOS T13, T14 on. This permits the elimination of a level-shifter in relation to the drive device of Figure 1, as every level-shifter comprises in addition to the output signal its negated signal, but it is necessary to add a circuitry to keep the transistors MOS not involved in the commutation during the abovementioned frame off; a decrease of the current used in the drive device of the columns derives from this. Therefore the device of Figure 5 also comprises a turnoff circuitry 15 capable of generating two signals tr-state1 and tr-state2 suitable for turning off, alternately through the level-shifters 11 and 12, the transistors PMOS T11, T12 or the transistors NMOS T13, T14 not involved in the commutations with the succession of the frame.

The signal LOW_FRAME is a logic signal that equals 0 in the even frames, and equalling 1 in the uneven frames. WHITE_PIX is instead a logic signal that equals 0 when the pixel has to be on, equalling 1 when the pixel has to be kept off. Starting from these two signals, through the circuit 10, the logic signals CP, CP_N, CN, CN_N, suitable for driving the level-shifters 11 and 12 are generated, which in turn drive the couple of transistors PMOS T11, T12 and the couple of transistors NMOS T13, T14.

The circuit 10 ensures that if the logic signal LOW_FRAME is at the logic level 1, the signals CP and CP_N are placed at the logic level 0 and the signals CN and CN_N commutate following the commutation of the signal WHITE_PIX; more precisely the signal CN is in phase with the signal WHITE_PIX while the signal CN_N is the signal CN negated.

Given that the logic signals CP and CP_N are at the logic level 0, the level-shifter 11 that is driven by said signals must be inactive so that the transistors PMOS T11 and T12 are off. In this case the signal tr-state1 generated by the circuitry 15 keeps the level-shifter 11 inactive. The transistors NMOS T13, T14 are driven by the level-shifter 12 which is operating and the output OUT of the column drive device varies between VSS and VB.

Again the circuit 10 ensures that if the logic signal LOW_FRAME is at the logic level 0, the signals CN and CN_N are placed at the logic level 1 and the signals CP and CP_N commutate following the commutations of the signal WHITE_PIX; more precisely the signal CP is in phase with the signal WHITE_PIX while the signal CP_N is the signal CP negated.

Given that the logic signals CN and CN_N are at the logic level 1, the level-shifter 12 that is driven by said signals must be inactive so that the transistors NMOS T13 and T14 are off. In this case the signal tr-state2 generated by the circuitry 15 keeps the level-shifter 12 inactive. The transistors PMOS T11, T12 are driven by the level-shifter 11 operating and the output OUT of the column drive device varies between VLCD and VA.

Figure 7 shows the temporal diagrams of the signals LOW_FRAME, WHITE_PIX, CN, CN_N, CP, CP_N, OUT that derive from simulations relating to two successive frames, that is an even frame and an uneven frame.

Figure 6 shows the components of the column drive device of Figure 5 more in detail.

The low voltage logic circuitry 10 comprises several gates NOT, NAND and NOR which starting from the signals WHITE_PIX and LOW_FRAME in input to the circuitry 10 generate the logic signals CP, CP_N, CN, CN_N, suitable for driving the level-shifters 11 and 12 and having a voltage value equal to the voltage VDD or to the voltage VSS as shown in Figure 6.

The device 11 comprises two transistors NMOS M8 and M9 driven by the signals CP and CP_N whose source terminals are connected to the voltage VSS and whose drain terminals are connected respectively to the drain terminals of two transistors PMOS M4 and M5 on the source terminal of which the voltage VLCD is present. The gate terminals of the transistors M4 and M5 are connected to the drain terminals of the transistors M9 and M8.

The same drain terminals of the transistors M8 and M9 are connected to the gate terminals of the transistors M2 and M1 on the source terminals of which the voltage VLCD is present, and at the drain terminals of the transistors M3 and M6 on the source terminals the voltage VLCD is present. The transistors M1, M2, M3, M6 belong to the turnoff circuitry 15 that also comprises a transistor M7 having its source terminal connected to the voltage VSS, the drain terminal in common with the gate terminal of the transistors M3 and M6 and with the drain terminals of the transistors M1 and M2; the signal LOW_FRAME is present on the gate terminal.

The device 12 comprises two transistors NMOS M14 and M15 driven by the signals CN and CN_N whose source terminals are connected to the voltage VSS and whose drain terminals are connected respectively to the drain terminals of two transistors PMOS M12 and M13 the gate terminals of which are connected to the drain terminals of the transistors M15 and M14. The source terminals of the transistors M12 and M13 are connected to the drain terminals of two transistors M10 and M11 having the gate terminals in common and the voltage VLCD is present on the source terminals. The gate terminal of the transistors M10 and M11 is connected to the gate terminal of the transistor M6.

The pair of transistors PMOS T11 and T12 has a supply path between the voltages VLCD and VA while the couple of transistors NMOS T13 and T14 has a supply path between the voltages VB and VSS. The gate terminals of the transistors T11 and T12 are connected with the drain terminals of the

transistors M8 and M9 of the device 11 while the gate terminals of the transistors T13 and T14 are connected with the drain terminals of the transistors M15 and M14 of the device 12. The output terminal of the transistors T11 and T12 is connected to the output terminal of the transistors T13 and T14 and represents the output terminal OUT of the drive device of the present invention.

The circuit 10 ensures that, as it can be seen in Figure 6, if the logic signal LOW_FRAME is at the logic level 1, the signals CP and CP_N are placed at the logic level 0 and the signals CN and CN_N commutate following the commutations of the signal WHITE_PIX; more precisely the signal CN is in phase with the signal WHITE_PIX while the signal CN_N is the signal CN negated.

With the logic signals CP and CP_N at the logic level 0, the level-shifter 11 is inactive and the transistors PMOS T11 and T12 are off. In fact the transistor M7 is on and causes the transistors M3 and M6 to turn on as it brings the voltage on their gate terminals at VSS; in this manner the voltage on the gate terminals of the transistors T11 and T12 is brought to a voltage that is substantially the same as VLCD by means of the transistors M3 and M6. The turning on of the transistor M7 causes the transistors M10 and M11 to turn on, bringing the voltage on the source terminals of the transistors M12 and M13 practically the same as VLCD. In this case the signal tr-state1 generated by circuitry 15 is high and keeps the level-shifter 11 inactive; the signal tr-state2 is low and permits the device 12 to turn on. The transistors NMOS T13, T14 are driven by the level-shifter 12 operating and the output OUT of the column drive device varies between VSS and VB.

Again the circuit 10 ensures that if the logic signal LOW_FRAME is at the logic level 0, the signals CN and CN_N are placed at the logic level 1 and the signals CP and CP_N commutate following the commutations of the signal WHITE_PIX; more precisely the signal CP is in phase with the signal WHITE_PIX while the signal CP_N is the signal CP negated.

With the logic signals CN and CN_N at the logic level 1, the level-shifter 12 is inactive and the transistors NMOS T13 and T14 are off. In fact the transistor M7 is off and the turning on of one of the transistors M8 or M9 causes one of the transistors M2 o M1 to turn on as it brings the voltage on their gate terminals to VSS; in this manner the voltage on one of the gate terminals of the transistors T11 and T12 is brought to a voltage which is substantially equal to VSS. The turning on of one of the transistors M1 or M2 causes the transistors M3 and M6 to turn off and the transistors M10 and M11 that inhibit the turning on of the device 12 and of the transistors T13 and T14 to turn off. In this case the signal tr-state2 generated by the circuitry 15 is high and keeps the level-shifter 12 inactive; the signal tr-state1 is low and permits the device 11 to turn on. The transistors PMOS T11, T12 are driven by the level-shifter 11 operating and the output OUT of the column drive device varies between VLCD and VA.

CLAIMS

1. System for driving columns of a liquid crystal display comprising a logic circuitry (10) operating in a supply path between a first (VDD) and a second (VSS) supply voltage with said first supply voltage (VDD) higher than said second supply voltage (VSS), said logic circuitry (10) being capable of generating starting from the first logic signals (LOW_FRAME, WHITE_PIX) in input second logic signals (CP, CN, CP_N, CN_N) in output whose value is equal to said first (VDD) or second (VSS) supply voltage, elevator devices (11, 12) coupled to said logic circuitry (10) and operating in a supply path between a third supply voltage (VLCD) greater than said first supply voltage (VDD) and said second supply voltage (VSS), said elevator devices (11, 12) being capable of raising the value of said second logic signals (CP, CN, CP_N, CN_N), a first (T11-T12) and a second (T13-T14) pair of transistors having different supply paths (VLCD-VA, VB-VSS) and having an output terminal (OUT) in common, said first (T11-T12) and second (T13-T14) pair of transistors being associated to said elevator devices (11, 12) and a said logic circuitry (10) so as to determine the drive signal of a column, characterised in that said elevator devices (11, 12) are two and each of them is connected with one of said pairs of transistors (T11-T12, T13-T14), and in that it comprises turnoff circuitry (15) coupled to said two elevator devices (11, 12), said circuitry (10) being capable of keeping one of said two pairs of transistors (T11-T12, T13-T14) in the turnoff state in the period of time of a frame when the other of said two pairs of transistors (T11-T12, T13-T14) is in operative conditions.

2. Device according to claim 1, characterised in that said turnoff circuitry (15) operates in a supply path between said third (VLCD) and said second supply voltage (VSS)

3. Device according to claim 1, characterised in that each of said two elevator devices (11, 12) drives separately the transistors of one of said pairs (T11-T12, T13-T14) of transistors.

4. Device according to claim 3, characterised in that said turnoff circuitry (15) has one (LOW_FRAME) of said first logic signals (LOW_FRAME, WHITE_PIX) in input whose value changes according to an even frame or an uneven frame.

5. Device according to claim 4, characterised in that said turnoff circuitry (15) sends two signals (tr_state1, tr_ state2) complementary with each other respectively to said two elevator devices (11, 12) according to the state of said logic signal (LOW_FRAME) in input so as to inhibit the turning on of one or the other elevator device .

6. Device according to claim 5, characterised in that said pairs of transistors (T11-T12, T13-T14) are pairs of transistors MOS.

7. Device according to claim 6, characterised in that said pairs of transistors MOS (T11-T12, T13-T14) are made up of a pair of transistors PMOS (T11-T12) and of a pair of transistors NMOS (T13-T14), and said two elevator devices (11, 12) each comprise a first (M8, M14) and a second (M9, M15) transistor NMOS driven by two of said second logic signals (CP, CN, CP_N, CN_N) complementary between each other and a first (M4, M12) and a second (M5, M13) transistor PMOS having the terminals that can be driven connected respectively with the drain terminal of said second (M9, M15) and first (M8, M14) transistor NMOS, the drain terminals connected respectively with the drain terminals of said first (M8, M14) and second (M9, M15) transistor NMOS, and the source terminals coupled with said third supply voltage (VLCD).

8. Device according to claim 7, characterised in that said turnoff circuitry (15) comprises a first transistor (M7) on whose terminal that can be driven said logic signal (LOW_FRAME) in input is present and having a terminal that cannot be driven connected to said second supply voltage (VSS) and the other terminal that cannot be driven connected to the terminals that can be driven of two additional transistors (M3, M6) having first terminals that cannot be driven connected respectively with the drain

terminals of said first (M8) and second (M9) transistor NMOS of one (11) of said elevator devices (11, 12) and the other terminal that cannot be driven connected with said third supply voltage (VLCD), the terminal that can be driven of said two additional transistors (M3, M6) being connected to the terminal that can be driven in common with two more additional transistors (M10, M11) having first terminals that cannot be driven connected respectively with the source terminals of said first (M12) and second (M13) transistor PMOS of the other of (12) said elevator devices (11, 12) and the other terminal that cannot be driven connected to the third supply voltage (VLCD), said circuitry (15) comprising two more additional transistors (M1, M2) having the terminals that can be driven connected respectively with the drain terminals of said first (M8) and second (M9) transistor NMOS of one (11) of said elevator devices (11, 12), first terminals that cannot be driven connected to said additional terminal that cannot be driven of said first transistor (M7) and second terminal that cannot be driven connected to said third supply voltage (VLCD).

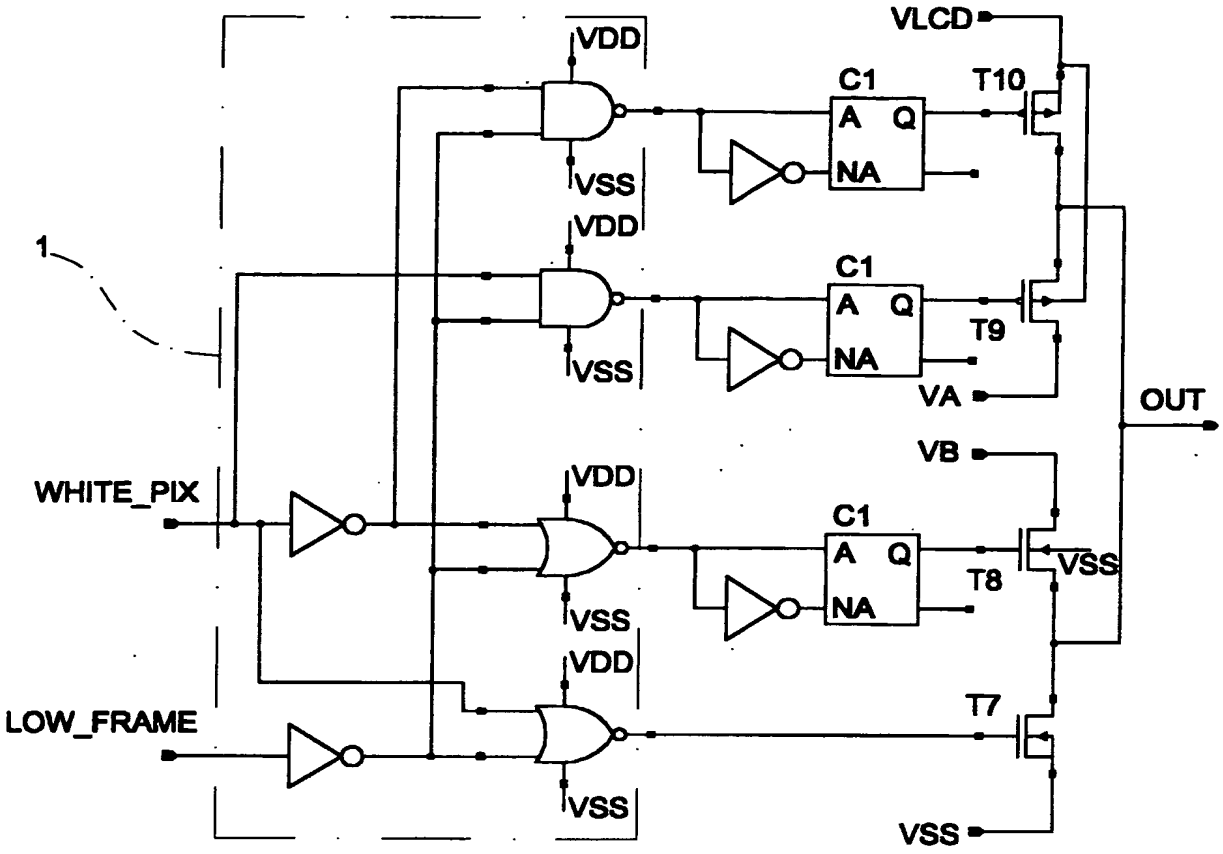

VLCD
VDD
C1
A Q
NA
T10
VSS
VDD
C1
A Q
NA
T9
VA
OUT
1
VB
WHITE_PIX
VDD
C1
A Q
NA
T8
VSS
VSS
VDD
T7
LOW_FRAME
VSS
VSS

Fig.1

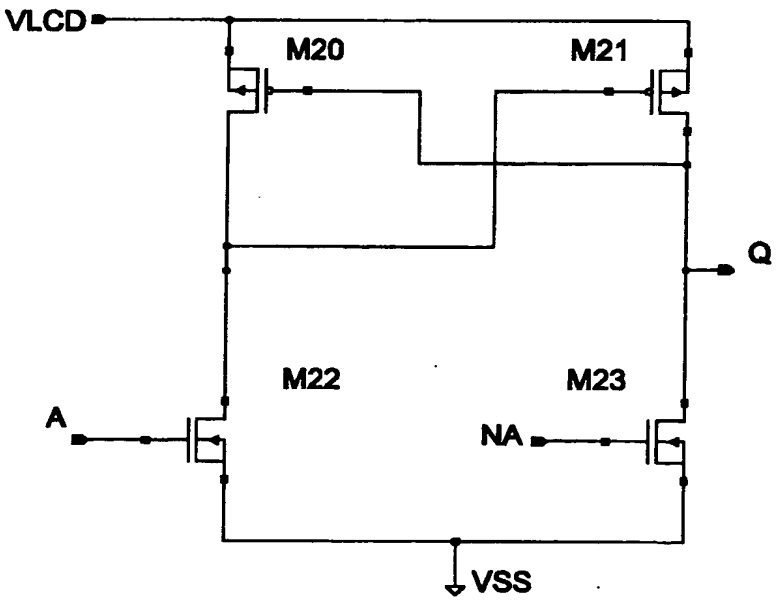

VLCD
M20
M21
Q
M22
M23
A
NA
VSS

Fig.2

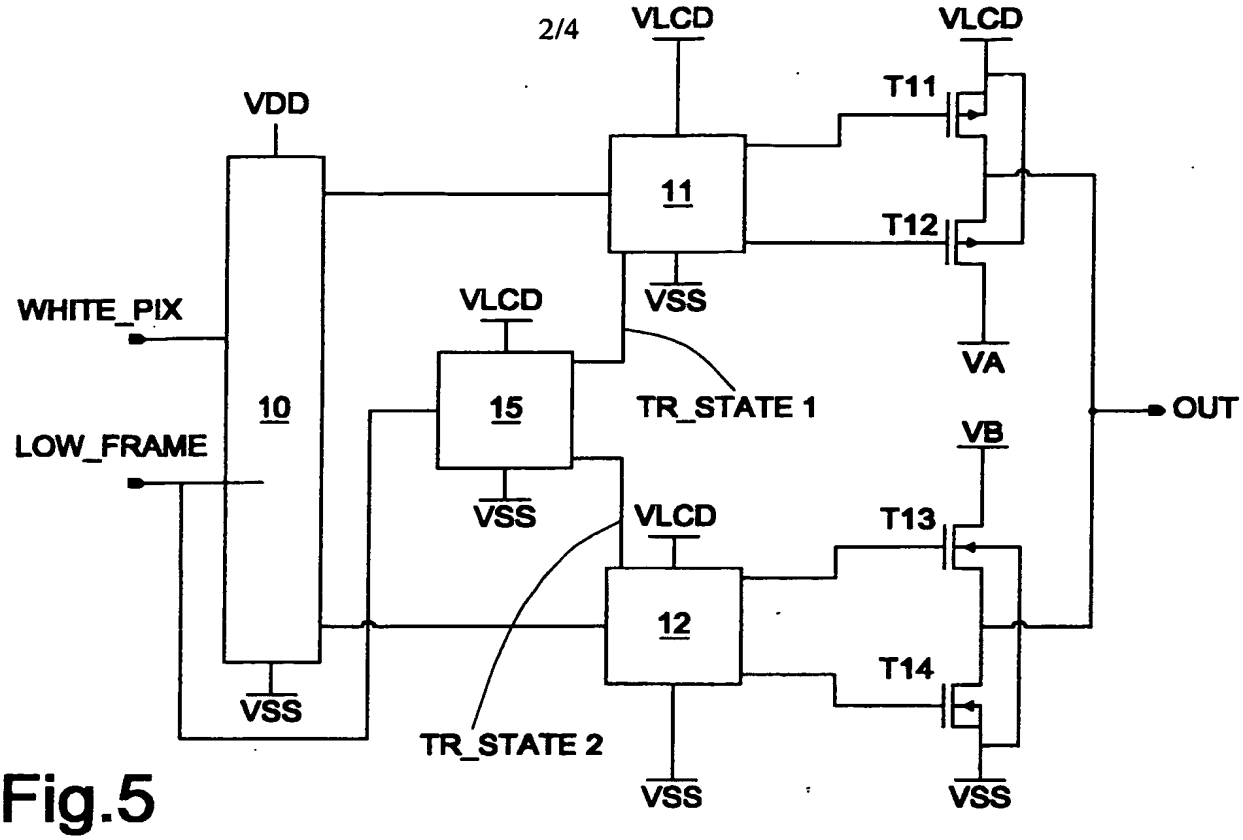
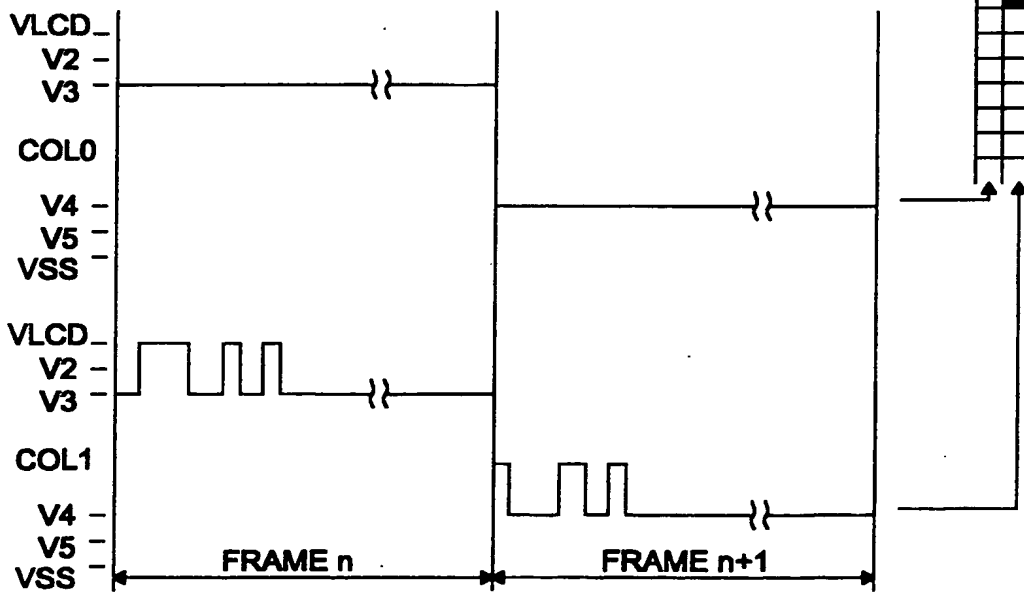


Fig.5

Fig.3



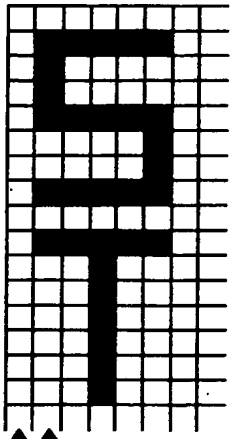


Fig.4

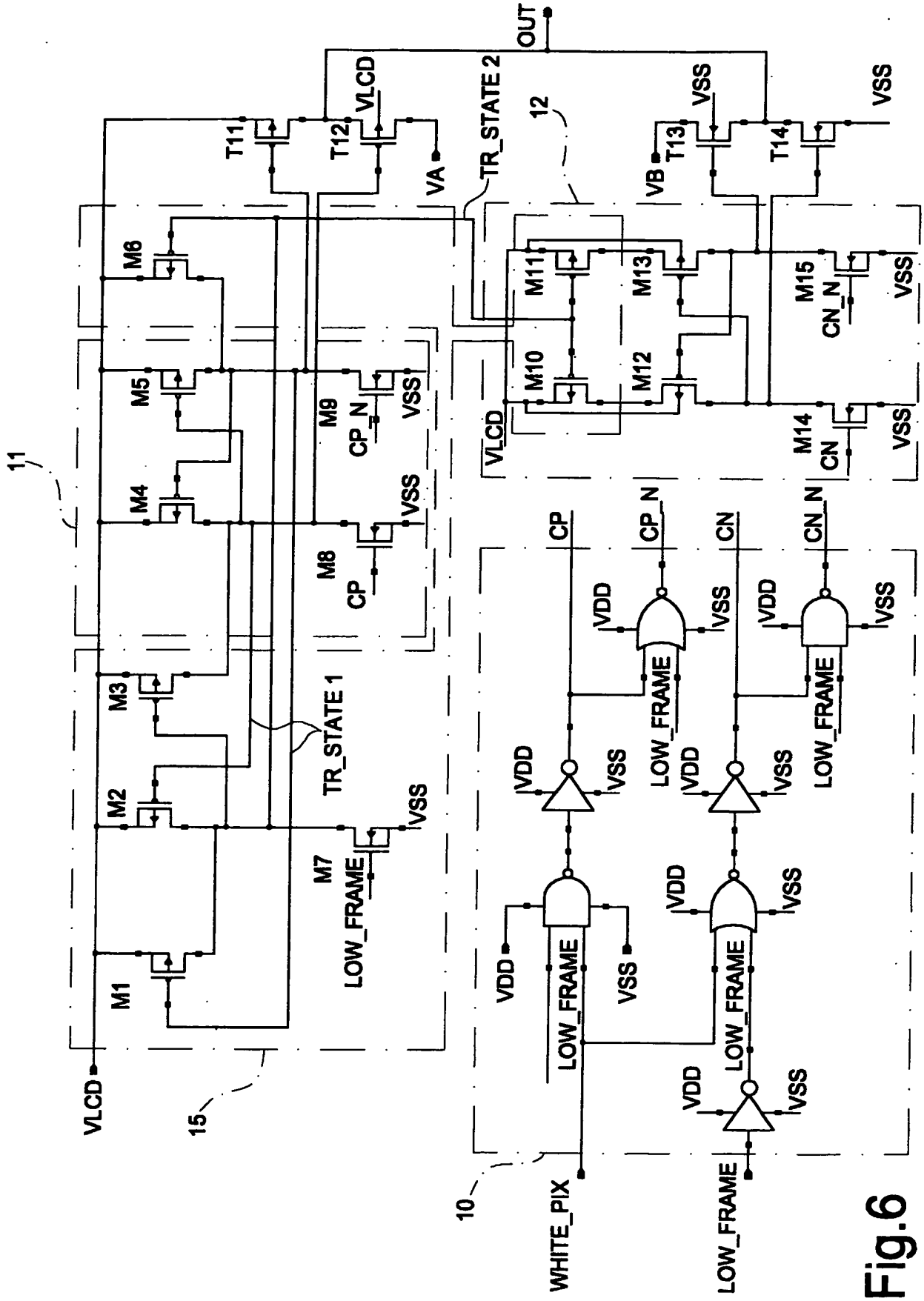

OUT
VLCD
T11
T12
VA
TR_STATE 2
12
VB
T13
T14
VSS
M6
M5
M4
M3
M2
M1
M9
CP_N
M8
CP
M7
LOW_FRAME
TR_STATE 1
11
15
VLCD
M11
M13
M15
CN_N
M10
M12
M14
CN
CP
CP_N
CN
CN_N
VDD
LOW_FRAME
10
WHITE_PIX
LOW_FRAME

Fig.6

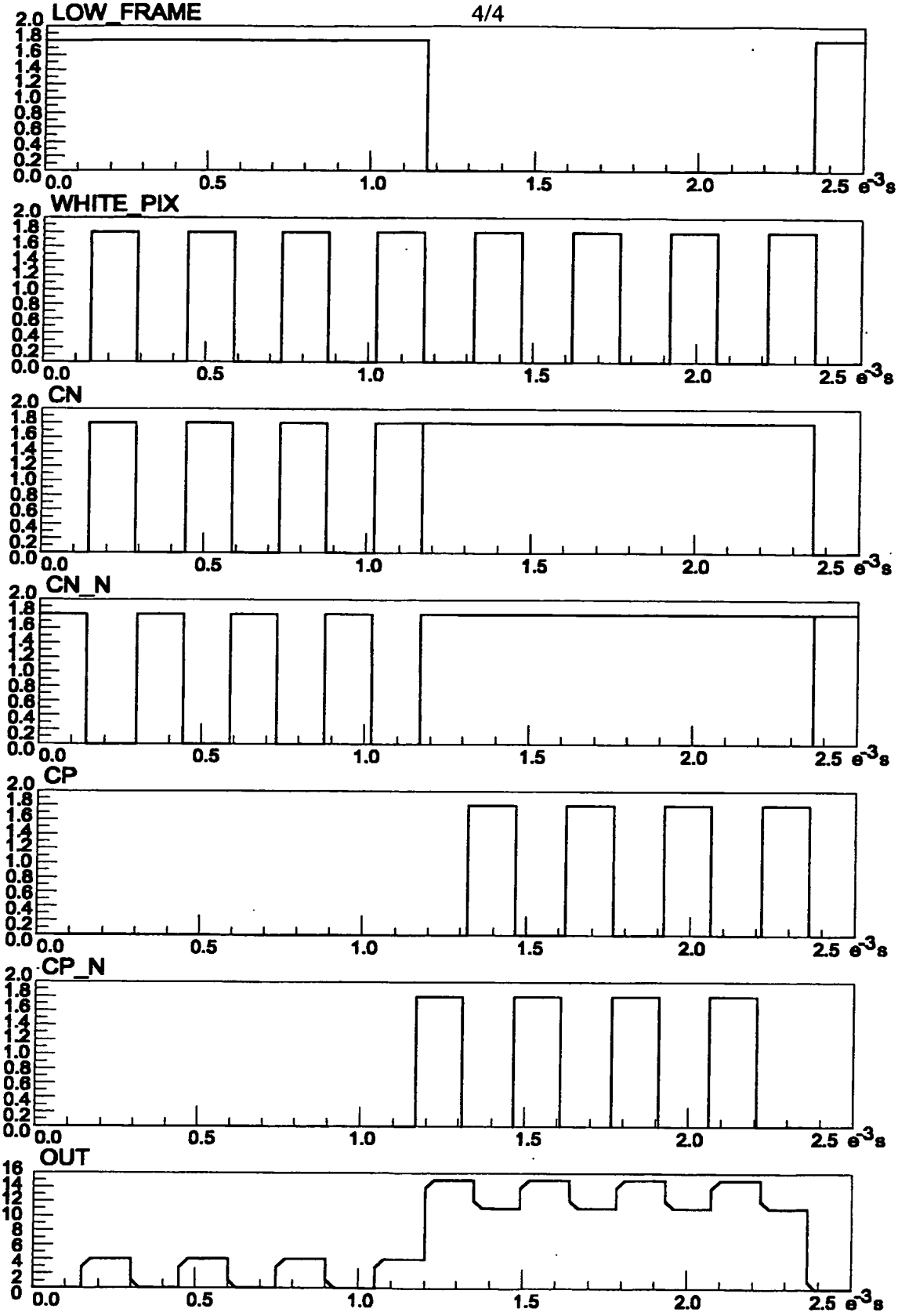


Fig.7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/[redacted]03/06638

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 11, 3 January 2001 (2001-01-03) -& JP 2000 221926 A (SONY CORP), 11 August 2000 (2000-08-11) abstract the whole document	1-8
P,X	US 2002/140686 A1 (MATSUMOTO SHOICHIRO ET AL) 3 October 2002 (2002-10-03)	1
A	abstract	4-8
Y	paragraph '0011! paragraph '0018! - paragraph '0024! paragraph '0053! - paragraph '0062!; figures 1-3	2,3

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 November 2003	25/11/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Wolff, L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Internat[redacted]pplication No
PCT/[redacted]03/06638

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
P,X	EP 1 265 217 A (SEIKO EPSON CORP) 11 December 2002 (2002-12-11) abstract	1
Y	paragraph '0105! - paragraph '0112!; figures 11A,11B	2,3
A	paragraph '0165! - paragraph '0182!; figure 18	4-8
A	US 5 731 795 A (KANDA SHOJI ET AL) 24 March 1998 (1998-03-24) abstract the whole document	1-8

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/[redacted]3/06638

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2000221926 A	11-08-2000	EP 1014334 A2	28-06-2000
		KR 2000052541 A	25-08-2000
		TW 461180 B	21-10-2001
US 2002140686 A1	03-10-2002	JP 2002358058 A	13-12-2002
EP 1265217 A	11-12-2002	JP 2002366104 A	20-12-2002
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